Features

- **Full Range of Matrices with up to 480K Gates**
- **0.5 µm Drawn CMOS, 3 Metal Layers, Sea of Gates**
- **RAM and DPRAM Compilers**
- **Library Optimized for Synthesis, Floor Plan and Automatic Test Generation (ATG)**
- **3 and 5 Volts Operation; Single or Dual Supply Mode**
- **High Speed Performances:**
  - **450 ps Max NAND2 Propagation Delay at 4.5V, 720 ps at 2.7V and FO = 5**
  - **Min 610 MHz Toggle Frequency at 4.5V, 320 MHz at 2.7V**
- **Programmable PLL Available upon Request**
- **High System Frequency Skew Control through Clock Tree Synthesis Software**
- **Low Power Consumption:**
  - **1.96 µW/Gate/MHz at 5V**
  - **0.6 µW/Gate/MHz at 3V**
- **Integrated Power On Reset**
- **Matrices with a Max of 484 Fully Programmable Pads**
- **Standard 3, 6, 12 and 24 mA I/Os**
- **Versatile I/O Cell: Input, Output, I/O, Supply, Oscillator**
- **CMOS/TTL/PCI Interface**
- **ESD (2 kV) and Latch-up Protected I/O**
- **High Noise and EMC Immunity:**
  - **I/O with Slew Rate Control**
  - **Internal Decoupling**
  - **Signal Filtering between Periphery and Core**
  - **Application Dependent Supply Routing and Several Independant Supply Sources**
- **Wide Selection of MQFPs and MCGA Packages up to 472 Pins**
- **Delivery in Die Form with 94.6 µm Pad Pitch**
- **Advanced CAD Support: Floor Plan, Proprietary Delay Models, Timing Driven Layout, Power Management**
- **Cadence®, Mentor®, Vital® and Synopsys® Reference Platforms**
- **EDIF and VHDL Reference Formats**
- **Available in Military and Space Quality Grades (SCC, MIL-PRF-38535)**
- **No Single Event Latch-up below an LET threshold of 80MeV/mg/cm^2**
- **Tested up to a Total Dose of 60 Krad (Si) according to MIL STD 883 Method 1019**
- **QML Q and V with SMD 5962-00B02**

Description

The MG2RT series is a 0.5 micron, array based, CMOS product family. Several arrays up to 480K gates cover most system integration needs. The MG2RT is manufactured using a 0.5 micron drawn, 3 metal layer CMOS process, called SCMOS 3/2RT.

The base cell architecture of the MG2RT series provides high routability of logic with extremely dense compiled memories: RAM and DPRAM. ROM can be generated using synthesis tools.

Accurate control of clock distribution can be achieved by PLL hardware and CTS (Clock Tree Synthesis) software. New noise prevention techniques are applied in the array and in the periphery: three or more independent supplies, internal decoupling, customiszation dependent supply routing, noise filtering, skew controlled I/Os, low swing differential I/Os, all contribute to improve the noise immunity and reduce the emission level.

The MG2RT is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Verilog, Modelsym and Design Compiler are the reference front-end tools. Floor planning associated with timing-driven layout provides a short back-end cycle.

Rad Tolerant 350K Used Gates 0.5 µm CMOS Sea of Gates

MG2RT

The MG2RT library allows straight forward migration from the MG1RT and MG1 Sea of Gates.

A netlist based on this library can be simulated as either MG2RT or MG2RTP. It can also be simulated as MG2 provided there are no SEU hardened cells.

Table 1. List of Available MG2RT Matrices

Type	Total Gates	Typical Usable Gates	Total Pads	Maximum Programmable I/O
MG2044E (1)	44616	31200	173	150
MG2091E	91464	64000	237	214
MG2194E (1)	193800	135600	333	310
MG2265E	264375	185000	385	362
MG2360E (1)	361680	253100	445	422
MG2480E	481143	336800	507	484

Note: Not available for new designs.

Libraries

The MG2RT cell library has been designed to take full advantage of the features offered by both logic and test synthesis tools.

Design testability is assured by the full support of SCAN, JTAG (IEEE 1149) and BIST methodologies.

More complex macro functions are available in VHDL, such as Two-wire Interface (TWI), UART, Timer.

Block Generators

Block generators are used to create a customer specific simulation model and metallisation pattern for regular functions like RAM and DPRAM. The basic cell architecture allows one bit per cell for RAM and DPRAM. The main characteristics of these generators are summarised below.

Function	Maximum Size (bits)	Bits/Word	Typical Characteristics (16 Kbits) at 5V	
			Access Time (ns)	Used Cells
RAM	32K	1-36	8.6	20K
DPRAM	32K	1-36	9.2	23K

I/O Buffer Interfacing

I/O Flexibility

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator is located close to each buffer.

Inputs

Input buffers with CMOS or TTL thresholds are non-inverting and feature versions with and without hysteresis. The CMOS and TTL input buffers may incorporate pull-up or pull down terminators. For special purposes, a buffer allowing direct input to the matrix core is available.

Outputs

Several kinds of CMOS and TTL output drivers are offered: fast buffers with 3, 6, 12 and 24 mA drive at 5V, low noise buffers with 12 mA drive at 5V.

Clock Generation and PLL

Clock Generation

Atmel offers 6 different types of oscillators: 4 high frequency crystal oscillators and 2 RC oscillators. For all devices, the mark-space ratio is better than 40/60 and the start-up time less than 10 ms.

Oscillators	Frequency (MHz)		Typical Consumption (mA)	
	Max 5V	Max 3V	5V	3V
Xtal 7M	12	7	1.2	0.4
Xtal 20M	28	17	2.5	0.8
Xtal 50M	70	40	7	2
Xtal 100M	130	75	16	5
RC 10M	10	10	2	1
RC 32M	32	32	3	1.5

PLL

Contact factory.

Power Supply and Noise Protection

The speed and density of the SCMOS3/2RT technology cause large switching current spikes for example when:

- either 16 high current output buffers switch simultaneously,
- or 10% of the 480,000 gates are switching within a window of 1 ns.

Sharp edges and high currents cause some parisitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the settling time of the current and causes voltage drops on the power supply lines. These drops can affect the behavior of the circuit itself or disturb the external application (ground bounce).

In order to improve the noise immunity of the MG core matrix, several mechanisms have been implemented inside the MG arrays. Two kinds of protection have been added: one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

I/O Buffers Switching Protection

Three features are implemented to limit the noise generated by the switching current:

- The power supplies of the input and output buffers are separated.
- The rise and fall times of the output buffers can be controlled by an internal regulator.
- A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix Switching Current Protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added:

- Decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.
- A power supply network has been implemented in the matrix. This solution reduces the number of parasitic elements such as inductance and resistance and constitutes an artificial VDD and Ground plane. One mesh of the network supplies approximately 150 cells.
- A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the VDD supply of the matrix to the external world via the output buffers.

Packaging

Atmel offers a wide range of packaging options which are listed below:

Package Type[1]	Pins min/max	Lead Spacing (mils)
MQFP	100	25
	132	25
	196	25
	256	20
	352	20

Note: 1. Contact Atmel local design centers to check the availability of the matrix/package combination.

Design Flows and Tools

Design Flows and Modes

A generic design flow for an MG2RT array is illustrated below.

A top down design methodology is proposed which starts with high level system description and is refined in successive design steps. At each step, structural verification is performed which includes the following tasks:

- Gate level logic simulation and comparison with high level simulation results.
- Design and test rules check.
- Power consumption analysis.
- Timing analysis (only after floor plan).

The main design stages are:

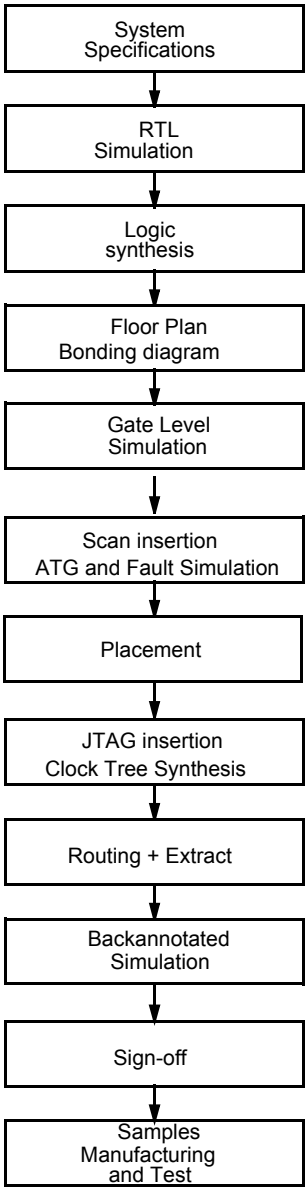
- System specification, preferably in VHDL form.
- Functional description at RTL level.
- Logic synthesis.
- Floor planning and bonding diagram generation.
- Test/Scan insertion, ATG and/or fault simulation.
- Physical cell placement, JTAG insertion and clock tree synthesis.
- Routing.

To meet the various requirements of designers, several interface levels between the customer and Atmel are possible.

For each of the possible design modes a review meeting is required for data transfer from the user to Atmel. In all cases the final routing and verifications are performed by Atmel.

The design acceptance is formalized by a design review which authorizes Atmel to proceed with sample manufacturing.

Figure 1. MG2RT Design Flow



Design Tool and Design Kits (DK)

The basic content of a design kit is described in the table below.

The interface formats to and from Atmel rely on IEEE or industry standard:

- VHDL for functional descriptions
- VHDL or EDIF for netlists
- Tabular, log or .VCD for simulation results
- SDF (VITAL format) and SPF for back annotation
- LEF and DEF for physical floor plan information

The design kits supported for several commercial tools are listed below.

Design Kit Support

- Cadence/Verilog (RTL and gate), Logic Design Planner
- Mentor/Modelsim (RTL and gate), Velocity, BSD Architect, Flex Test
- Synopsys, Design Compiler, PrimeTime
- Vital

Table 2. Design Kit Description

Design Tool or library	Atmel Software Name	Third Party Tools
Design manual and libraries		(1)
Synthesis library		(1)
Gate level simulation library		(1)
Design rules analyser	STAR	
Power consumption analyser	COMET	
Floor plan library		(1)
Timing analyser library		(1)
Package and bonding software	PIM	
Scan path and JTAG insertion		(1)
ATG and fault simulation library		(1)

Note: 1. Refer to “Design kits cross reference tables” ATD-TS-WF-R0181

Electrical Characteristics

Absolute Maximum Ratings

Ambient temperature under bias (TA)
Military ..... -55 to +125°C
Junction temperature..... TJ < 175°C
Storage temperature..... -65 to +150°C

TTL/CMOS:
Supply voltage VDD ..... -0.5V to +7V
I/O voltage .....-0.5V to VDD + 0.5V

Note: Stresses above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

DC Characteristics

Table 3. DC Characteristics - Specified at VDD = +5V ± 10%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW voltage (3) CMOS input TTL input	 0 0		 1.5 0.8	V	
VIH	Input HIGH voltage(3) CMOS input TTL input	 3.5 2.2		 VDD VDD	V	
VOL	Output LOW voltage			0.4	V	IOL =24, 12, 6, 3 mA(1)
VOH	Output HIGH voltage	3.9			V	IOL =-24, -12, -6, -3 mA(1)
VT+	Schmitt trigger positive threshold CMOS input TTL input			 3.6 1.8	V	
VT-	Schmitt trigger negative threshold CMOS input TTL input	 1.2 1.0			V	
Delta V	CMOS hysteresis 25°C/5V TTL hysteresis 25°C/5V		1.9 0.6		V	
IL	Input leakage No pull up/down Pull up Pull down	 -5 -55 79	 -69 125	 +5 -120 330	 µA µA µA	
IOZ	3-State Output Leakage current	-5		+5	µA	
IOS	Output Short circuit current IOSN IOSP			 90 180 270 540	 mA	 BOUT3 BOUT6 BOUT12 BOUT24
ICCSB	Leakage current per cell		1.0	10.0	nA	
ICCOP	Operating current per cell		0.39	0.58	µA/MHz/gate	

Notes:
1. According buffer: Bout24, Bout12, Bout6, Bout3.
2. Supplied as a design limit but not guaranteed or tested. No more than one output at a time may be shorted for a maximum duration of 10 seconds.
3. Without Schmitt trigger.

Table 4. DC Characteristics - Specified at VDD = +3V ± 0.3V

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW voltage[3] LVCMOS input LVTTL input	 0 0		 0.3 VDD 0.8	V	
VIH	Input HIGH voltage[3] LVCMOS input LVTTL input	 0.7 VDD 2.0		 VDD VDD	V	
VOL	Output LOW voltage LVTTL			0.4	V	IOL=12, 6, 3, 1.5 mA[1]
VOH	Output high voltage LVTTL	2.4			V	IOH= -8, -4, -2, -1 mA[1]
VT+	Schmitt trigger positive threshold LVCMOS input LVTTL input			 2.2 1.2	V	
VT-	Schmitt trigger negative threshold LVCMOS input LVTTL input	 0.9 0.8			V	
Delta V	CMOS hysteresis 25°C/3V TTL hysteresis 25°C/3V		0.8 0.2		V	
IL	Input leakage No pull up/down Pull up Pull down	 -1 -20 32	 24 42	 +1 -60 150	 µA µA µA	
IOZ	3-State Output Leakage current			±1	µA	
IOS	Output Short circuit current IOSN IOSP			 90 180 270 540	mA	 BOUT3 BOUT6 BOUT12 BOUT24
ICCSB	Leakage current per cell		0.6	5	nA	
ICCOP	Operating current per cell		0.2	0.25	µA/MHz/gate	

Notes:
1. According buffer: Bout24, Bout12, Bout6, Bout3.
2. Supplied as a design limit but not guaranteed or tested. No more than one output at a time may be shorted for a maximum duration of 10 seconds.
3. Without Schmitt trigger.

AC Characteristics

Table 5. AC Characteristics - TJ = 25°C, Process typical (all values in ns)

Buffer	Description	Load	Transition	VDD	
				5V	3V
BOUT12	Output buffer with 12 mA drive	60 pf	Tplh	2.53	3.91
			Tphl	2.76	3.64
BOUT3	Output buffer with 3 mA drive	60 pf	Tplh	4.63	7.22
			Tphl	4.86	6.36
BOUTQ	Low noise output buffer with 12 mA drive	60 pf	Tplh	2.97	4.48
			Tphl	4.36	6.24
B3STA3	3-state output buffer with 3 mA drive	60 pf	Tplh	4.73	7.35
			Tphl	4.89	6.44
B3STA12	3-state output buffer with 12 mA drive	60 pf	Tplh	2.64	4.07
			Tphl	2.79	3.72
B3STAQ	Low noise 3-state output buffer with 12 mA drive	60 pf	Tplh	3.01	4.61
			Tphl	4.42	6.34

Table 6. AC Characteristics - TJ = 25°C, Process typical (all values in ns)

Cell	Description	Load	Transition	VDD	
				5V	3V
BINCMOS	CMOS input buffer	15 fan	Tplh	0.77	1.14
			Tphl	0.75	1.06
BINTTL	TTL input buffer	16 fan	Tplh	0.9	1.31
			Tphl	0.7	1.1
INV	Inverter	12 fan	Tplh	0.52	0.8
			Tphl	0.42	0.53
NAND2	2 - input NAND	12 fan	Tplh	0.73	1.11
			Tphl	0.66	0.9
FDFF	D flip-flop, Clk to Q	8 fan	Tplh	0.8	1.21
			Tphl	0.68	1.02
			Ts	0.33	0.44
			Th	-0.12	-0.24
BUF4X	High drive internal buffer	51 fan	Tplh	0.76	1.1
			Tphl	0.58	0.81
NOR2	2-Input NOR gate	8 fan	Tplh	0.65	1.08
			Tphl	0.37	0.45
OAI22	4-input OR AND INVERT gate	8 fan	Tplh	0.68	1.14
			Tphl	0.42	0.54
OSFF	D flip-flop with scan input, Clk to Q	8 fan	Tplh	0.83	1.23
			Tphl	1.00	1.38
			Ts	0.56	0.8
			Th	-0.34	-0.6

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